films **14** are formed to surround the low permittivity regions **15**, the sidewall films **14** each consisting of the first film **14***a* and the second film **14***b*.

[**0044**] Next, as shown in **FIG. 5G**, the ion implantation of the n-type impurity such as phosphorus (P) is performed using the gate electrode **13** and the sidewall films **14** as masks, and a source **17** and a drain **17** are formed on the surface layer of the semiconductor substrate **11** to partially overlap with the extension regions **16**.

[**0045**] Thereafter, interlayer insulation films, contact holes, various wiring layers, and the like are formed to bring the MOS transistor to completion.

[**0046**] Second Embodiment

[**0047**] **FIGS. 6A** to **6**F are schematic sectional views showing, in a process order, a method for manufacturing a MOS transistor relating to this embodiment.

[**0048**] First, as shown in **FIG. 6A**, a polycrystalline silicon film (not shown) is deposited on, for example, a p-type silicon semiconductor substrate **11** via a gate insulation film **12** by a CVD method or the like, and patterning of the polycrystalline silicon film and the gate insulation film **12** into an electrode shape causes to form a gate electrode **13**.

[**0049**] Next, as shown in **FIG. 6B**, for example, a silicon oxide film (not shown) is deposited on the semiconductor device **11** by the CVD method or the like to cover the gate electrode **13**, and full anisotropic etching (etch back) of this silicon oxide film causes to form thin first films **14***a* only on side surfaces of the gate electrode **13** and the gate insulation film **12**.

[**0050**] Next, as shown in **FIG. 6C**, only lower portions of the first films **14***a* are selectively removed by, for example, wet etching, to expose surfaces on side lower portions of the gate electrode **13**. Here, the exposed side lower portions of the gate electrode **13** become low permittivity regions **15**.

[**0051**] Next, as shown in **FIG. 6D**, ion implantation of an n-type impurity such as phosphorus (P) is performed using the gate electrode **13** and the first films **14***a* as masks, to form a pair of extension regions **16** on a surface layer of the semiconductor substrate **11**.

[**0052**] Next, a silicon oxide film (not shown) covering the gate electrode **13** and the first films **14***a* is formed with low step coverage (low in step coverage) to such an extent as not to fill in the low permittivity regions **15**. This silicon oxide film may be formed by a low temperature oxidation (LTO) method or a sputtering method. For example, it is formed under the condition of low temperature of 400 by inputting high frequency (RF) power of 400 W with the use of a parallel plate plasma CVD apparatus. Then, as shown in **FIG. 6E**, the full anisotropic etching (etch back) of this silicon oxide film causes to form second films **14***b* that cover the low permittivity regions **15**. Thereby, sidewalls **14** are formed to surround the low permittivity regions **15**, the sidewalls **14** covering the first films **14***a* to have a cavity **22** with the first film **14***a*.

[**0053**] Next, as shown in **FIG. 6F**, the ion implantation of the n-type impurity such as phosphorus (P) is performed using the gate electrode **13** and the sidewall films **14** as masks, and a source **17** and a drain **17** are formed on the surface layer of the semiconductor substrate **11** to partially overlap with the extension regions **16**.

[**0054**] Thereafter, interlayer insulation films, contact holes, various wiring layers, and the like are formed to bring the MOS transistor to completion.

[**0055**] Third Embodiment

[**0056**] **FIGS. 7A** to **7**F are schematic sectional views showing, in a process order, a method for manufacturing a MOS transistor relating to this embodiment.

[**0057**] First, as shown in **FIG. 7A**, a polycrystalline silicon film (not shown) is deposited on, for example, a p-type silicon semiconductor substrate **11** via a gate insulation film **12** by a CVD method or the like, and patterning of the polycrystalline silicon film and the gate insulation film **12** into an electrode shape causes to form a gate electrode **13**.

[**0058**] Next, as shown in **FIG. 7B**, side wall lower portions of the gate electrode **13** and a part of the gate insulation film **12** are removed by etching to make it notch-shaped. The notch sections become low permittivity regions **18**.

[**0059**] Next, as shown in **FIG. 7C**, ion implantation of an n-type impurity such as phosphorus (P) is performed using the gate electrode **13** as a mask, to form a pair of extension regions **16** on a surface layer of the semiconductor substrate **11**.

[**0060**] Next, as shown in **FIG. 7D**, a low permittivity material **23** is formed on the gate electrode **13** with the low permittivity regions **18** being filled in, and etching (for example, etch back) thereof causes to leave the low permittivity materials **23** only in the low permittivity regions **18**. Here, such low permittivity materials are used for the low permittivity material **23** as a SiOF, an arylether based organic low permittivity material, a fluorocarbon based low permittivity material, a hydrogen silses quioxane based low permittivity material, a hydromethyl silses quioxane based low permittivity material, a porous quioxane based low permittivity material, a porous allylether based low permittivity material, or the like.

[**0061**] Next, as shown in **FIG. 7E**, for example, a silicon nitride film (not shown) is deposited by the CVD method or the like to cover the gate electrode **13**, and thereafter the full anisotropic etching (etch back) of this silicon nitride film causes to form sidewall films **19** that cover side surfaces of the gate electrode **13** and the low permittivity regions **18** filled with the low permittivity material **23**.

[**0062**] Next, as shown in **FIG. 7F**, the ion implantation of the n-type impurity such as phosphorus (P) is performed using the gate electrode **13** and the sidewall films **19** as masks, and a source **17** and a drain **17** are formed on the surface layer of the semiconductor substrate **11** to partially overlap with the extension regions **16**.

[**0063**] Thereafter, interlayer insulation films, contact holes, various wiring layers, and the like are formed to bring the MOS transistor to completion.

[**0064**] Fourth Embodiment

[**0065**] **FIGS. 8A** to **8**E are schematic sectional views showing, in a process order, a method for manufacturing a MOS transistor relating to this embodiment.